

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	449	cache near test\$3 and @ad<"20040301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/11/14 18:18
L5	68	703/14.ccls. and @pd>"20070701"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/11/14 18:18


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

cache design test

1900

- 2004

Search

Ad
Sc
Sc
Scholar All articles - **Recent articles** Results 1 - 10 of about 35,000 for cache design test (0.39 sec)

All Results

[D Patterson](#)[J Hennessy](#)[C Su](#)[C Lee](#)[N Weste](#)
Cache design trade-offs for power and performance optimization: a case study

 CL Su, AM Despain - ... of the 1995 international symposium on Low power **design**, 1995 - portal.acm.org

 ... of Embedded Processors," IEEE **Design & Test** of Computers, Vol. 11, No. 4, pp. 24-31, Dec. 1994. [11] CL Su and Alvin M. Despain, "Cache Designs for Energy ...

 Cited by 206 - [Related Articles](#) - [Web Search](#)
Adaptive mode control: A static-power-efficient cache design - all 18 versions »

H Zhou, MC Toburen, E Rotenberg, TM Conte - ACM Transactions on Embedded Computing Systems (TECS), 2003 - portal.acm.org

 ... 3, August 2003. Page 11. Adaptive Mode Control: A Static-Power-Efficient **Cache Design** •

357 Table II. ... go 99 133 jpeg vigo.ppm 166 li test.lsp (queens 7) 202 ...

 Cited by 91 - [Related Articles](#) - [Web Search](#)
[book] Principles of CMOS VLSI design: a systems perspective - all 5 versions »

NHE Weste, K Eshraghian - 1985 - Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA

 ... on **Design**, automation and **test** in Europe, p.591-598, March 27-30, 2000, Paris, France. Tony D. Givargis , Jörg Henkel , Frank Vahid, Interface and **cache** power ...

 Cited by 1219 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
[book] Computer organization & design: the hardware/software interface - all 16 versions »

DA Patterson, JL Hennessy - 1993 - Morgan Kaufmann Publishers Inc. San Francisco, CA, USA

 ... Tony Givargis, Improved indexing for **cache** miss reduction in ... of the 40th conference on **Design** automation, June ... Instruction-level DFT for **testing** processor and ...

 Cited by 864 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
SimpleScalar: an infrastructure for computer system modeling - all 19 versions »

T Austin, E Larson, D Ernst - Computer, 2002 - ieeeexplore.ieee.org

 ... fast mechanism for **design** and **test** provides shorter ... Power-perfor- mance **design** tradeoff

 studies can be per ... issue width, instruction window size, **cache** size, and ...

 Cited by 448 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)
Scratchpad memory: design alternative for cache on-chip memory in embedded systems - all 13 versions »

R Banakar, S Steinke, BS Lee, M Balakrishnan, P ... - Proceedings of the tenth international symposium on Hardware ..., 2002 - portal.acm.org

 ... M Balakrishnan and P Marwedel, Comparison of **cache** and scratch ... Low power **design**


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Purchase History](#) |

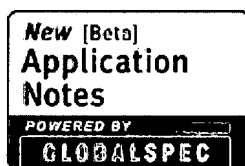
☐ Search Results

[BROWSE](#)
[SEARCH](#)
[IEEE XPLORE GUIDE](#)

Results for "((cache<near>simulate<and>test)) <and> (pyr >= 1913 <and> pyr <= 2004)"

Your search matched **2580** of **1685772** documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.



Modify Search

☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

» Search Options

[View Session History](#)
[New Search](#)

» Key



Indicates full text access

IEEE JNL IEEE Journal or Magazine
IET JNL IET Journal or Magazine
IEEE CNF IEEE Conference Proceeding
IET CNF IET Conference Proceeding
IEEE STD IEEE Standard

[IEEE/IET](#)
[Books](#)
[Educational Courses](#)
[A](#)

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and

[Select All](#) [Deselect All](#)

View: 1

- ☐ 1. **Verifying a multiprocessor cache controller using random test generatic**
 Wood, D.A.; Gibson, G.A.; Katz, R.H.;
Design & Test of Computers, IEEE
 Volume 7, Issue 4, Aug. 1990 Page(s):13 - 25
 Digital Object Identifier 10.1109/54.57906
[Abstract](#) | Full Text: [PDF\(920 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ 2. **A high performance IDDQ testable cache for scaled CMOS technologies**
 Bhunia, S.; Hai Li; Roy, K.;
Test Symposium, 2002. (ATS '02). Proceedings of the 11th Asian
 18-20 Nov. 2002 Page(s):157 - 162
 Digital Object Identifier 10.1109/ATS.2002.1181704
[Abstract](#) | Full Text: [PDF\(452 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
- ☐ 3. **IEEE recommended practice for futurebus+.**
 25 July 1994 Page(s):i
[Abstract](#) | Full Text: [PDF\(13404 KB\)](#) [IEEE STD](#)
- ☐ 4. **IVI comes of age: An overview of IVI specifications with current status**
 Bode, F.;
Aerospace and Electronic Systems Magazine, IEEE
 Volume 18, Issue 8, Aug 2003 Page(s):31 - 34
 Digital Object Identifier 10.1109/MAES.2003.1224970
[Abstract](#) | Full Text: [PDF\(311 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ 5. **An integrated functional performance simulator**
 Bechem, C.; Combs, J.; Utamaphethai, N.; Black, B.; Blanton, R.D.S.; Shen, .
Micro, IEEE
 Volume 19, Issue 3, May-June 1999 Page(s):26 - 35
 Digital Object Identifier 10.1109/40.768499